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L1	3618	(341/144,143,155).CCLS.	USPAT	OR	OFF	2005/06/22 09:35
L2	0	duyy cycle finite impulse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/06/22 09:36
L3	6	duty cycle finite impulse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/06/22 09:42
L4	10	duty cycle fir	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/06/22 09:42

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

1. **Characterization of pulse-modulated inductively coupled discharges in argon an**
Hebner, G.A.; Fleddermann, C.B.;
Plasma Science, 1997. IEEE Conference Record - Abstracts., 1997 IEEE International
19-22 May 1997 Page(s):141
AbstractPlus | Full Text: PDF(92 KB) IEEE CNF

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1 Technologies and devices for low-power: Characterizing and modeling minimum energy operation for subthreshold circuits

Benton H. Calhoun, Anantha Chandrakasan

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(373.68 KB) Additional Information: full citation, abstract, references, index terms

Subthreshold operation is emerging as an energy-saving approach to many new applications. This paper examines energy minimization for circuits operating in the subthreshold region. We show the dependence of the optimum V DD for a given technology on design characteristics and operating conditions. Solving equations for total energy provides an analytical solution for the optimum V DD and V T to minimize energy for a given frequency in subthreshold operation. SPICE simulations of a 200K transisto ...

Keywords: energy model, minimum energy point, subthreshold circuits, subthreshold model

2 Modeling and automating selection of guarding techniques for datapath elements

William E. Dougherty, Donald E. Thomas

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**

Full text available: pdf(734.33 KB) Additional Information: full citation, references, citings, index terms

Keywords: datapath energy modeling, guarded evaluation, low power design

3 A technique for testing command and control software

Marvin L. Watkins

April 1982 **Communications of the ACM**, Volume 25 Issue 4

Full text available: pdf(449.51 KB) Additional Information: full citation, abstract, references, citings, index terms

A technique for testing embedded-microprocessor command and control programs is described. The continuity inherent in functions computed by programs which monitor natural phenomena is exploited by a simple difference equation-based algorithm to predict

a program's next output from its preceding ones. The predicted output is compared with the actual output while indexing through the program's domain. Outputs which cannot be predicted are flagged as potential errors. Data are presented which ...

Keywords: predicator

4 On thermal effects in deep sub-micron VLSI interconnects
Kaustav Banerjee, Amit Mehrotra, Alberto Sangiovanni-Vincentelli, Chenming Hu
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(932.34 KB) Additional Information: full citation, references, citings, index terms

5 Application specific processors: A low power architecture for embedded perception
Binu Mathew, Al Davis, Mike Parker
September 2004 **Proceedings of the 2004 international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(310.49 KB) Additional Information: full citation, abstract, references, index terms

Recognizing speech, gestures, and visual features are important interface capabilities for future embedded mobile systems. Unfortunately, the real-time performance requirements of complex perception applications cannot be met by current embedded processors and often even exceed the performance of high performance microprocessors whose energy consumption far exceeds embedded energy budgets. Though custom ASICs provide a solution to this problem, they incur expensive and lengthy design cycles and ...

Keywords: VLIW, computer vision, embedded systems, low power design, perception, speech recognition, stream processor

6 Energy-efficient datapath scheduling using multiple voltages and dynamic clocking
Saraju P. Mohanty, N. Ranganathan
April 2005 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 10 Issue 2
Full text available: pdf(513.65 KB) Additional Information: full citation, abstract, references, index terms

Recently, dynamic frequency scaling has been explored at the CPU and system levels for power optimization. Low-power datapath scheduling using multiple supply voltages has been well researched. In this work, we develop new datapath scheduling algorithms that use multiple supply voltages and dynamic frequency clocking in a coordinated manner in order to reduce the energy consumption of datapath circuits. In dynamic frequency clocking, the functional units can be operated at different frequencies ...

Keywords: High-level synthesis, dynamic frequency clocking, low-power datapath synthesis, multiple voltage scheduling, resource-constrained scheduling, time-constrained scheduling

7 Smart Memories: a modular reconfigurable architecture
Ken Mai, Tim Paaske, Nuwan Jayasena, Ron Ho, William J. Dally, Mark Horowitz
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2
Full text available: pdf(80.16 KB) Additional Information: full citation, abstract, references, citings, index terms

Trends in VLSI technology scaling demand that future computing devices be narrowly

focused to achieve high performance and high efficiency, yet also target the high volumes and low costs of widely applicable general purpose designs. To address these conflicting requirements, we propose a modular reconfigurable architecture called Smart Memories, targeted at computing needs in the 0.1&mgr; technology generation. A Smart Memories chip is made up of many processing tiles, each containing local ...

8 Low power signal processing architectures for network microsensors
Michael J. Dong, K. Geoffrey Yung, Wiliam J. Kaiser
August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**
Full text available: pdf(613.09 KB) Additional Information: full citation, references, citings

9 A way-halting cache for low-energy high-performance systems
Chuanjun Zhang, Frank Vahid, Jun Yang, Walid Najjar
March 2005 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 2 Issue 1
Full text available: pdf(1.32 MB) Additional Information: full citation, abstract, references, index terms

Caches contribute to much of a microprocessor system's power and energy consumption. Numerous new cache architectures, such as phased, pseudo-set-associative, way predicting, reactive-associative, way-shutdown, way-concatenating, and highly-associative, are intended to reduce power and/or energy, but they all impose some performance overhead. We have developed a new cache architecture, called a way-halting cache, that reduces energy further than previously mentioned architectures, while imposing ...

Keywords: Cache, dynamic optimization, embedded systems, low energy, low power

10 Managing trust between collaborating companies using outsourced role based access control
Thomas Hildmann, Jörg Barholdt
October 1999 **Proceedings of the fourth ACM workshop on Role-based access control**
Full text available: pdf(885.42 KB) Additional Information: full citation, references, citings, index terms

11 Applications: Energy-efficient signal processing using FPGAs
Seonil Choi, Ronald Scrofano, Viktor K. Prasanna, Ju-Wook Jang
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Full text available: pdf(245.07 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present techniques for energy-efficient design at the algorithm level using FPGAs. We then use these techniques to create energy-efficient designs for two signal processing kernel applications: fast Fourier transform (FFT) and matrix multiplication. We evaluate the performance, in terms of both latency and energy efficiency, of FPGAs in performing these tasks. Using a Xilinx Virtex-II as the target FPGA, we compare the performance of our designs to those from the Xilinx library ...

Keywords: FFT, FPGA, energy efficient design techniques, matrix multiplicaiton, performance estimation

12 Geometry and positioning: Error characteristics of ad hoc positioning systems (aps)

Dragoş Niculescu, Badri Nath
May 2004 **Proceedings of the 5th ACM international symposium on Mobile ad hoc networking and computing**

Full text available: pdf(278.97 KB) Additional Information: full citation, abstract, references, citings, index terms

APS algorithms use the basic idea of distance vector routing to find positions in an ad hoc network using only a fraction of landmarks, for example GPS enabled nodes. All the nodes in the network are assumed to have the possibility of measuring: range, angle of arrival (AOA), orientation, or a combination of them. We give a lower bound for positioning error in a multihop network for a range/angle free algorithm, and examine the error characteristic of four classes of multihop APS algorithms unde ...

Keywords: APS, Cramér-rao lower bound, ad hoc networks, ad hoc positioning system, error analysis, multihop positioning

13 Session D: Link layer: Low power rendezvous in embedded wireless networks
Terry Todd, Frazer Bennett, Alan Jones
November 2000 **Proceedings of the 1st ACM international symposium on Mobile ad hoc networking & computing**

Full text available: pdf(996.70 KB) Additional Information: full citation, abstract, references, citings

In the future, wireless networking will be embedded into a wide variety of common, everyday objects [1]. In many embedded networking situations, the communicating nodes will be very small and battery powered. For this reason, it is crucial that power consumption is as low as possible. A technique for reducing power consumption is to place nodes into a *sleep mode* whenever possible, and have them occasionally awaken to interact with other nodes. This type of action is referred to as a node ...

14 What makes professionals so difficult: an investigation into professional ethics teaching
David Preston
June 1998 **ACM SIGCAS Computers and Society , Proceedings of the ethics and social impact component on Shaping policy in the information age**, Volume 28 Issue 2

Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references, citings, index terms

Teaching ethics to professionals pursuing a university degree programme requires a method that engages them with the realities and problematic nature of their workplace environment. In this paper we examine some of the history of Professional Ethics from a philosophical and political standpoint. Unfortunately this analysis appears to produce more questions than answers with the terms professional and expert seemingly poorly defined. In order to demonstrate some of the generic problems likely to ...

15 Data replicas in distributed information services
H. M. Gladney
March 1989 **ACM Transactions on Database Systems (TODS)**, Volume 14 Issue 1

Full text available: pdf(1.94 MB) Additional Information: full citation, abstract, references, index terms, review

In an information distribution network in which records are repeatedly read, it is cost-effective to keep read-only copies in work locations. This paper presents a method of updating replicas that need not be immediately synchronized with the source data or with each other. The method allows an arbitrary mapping from source records to replica records. It is fail-safe, maximizes workstation autonomy, and is well suited to a network with slow, unreliable, and/or expensive communications links ...

16 CAD: High level techniques for power-grid noise immunity
Azadeh Davoodi, Vishal Khandelwal, Ankur Srivastava
April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available: pdf(198.32 KB) Additional Information: full citation, abstract, references, index terms

Power-grid networks are very important aspects of large scale integrated systems. In the modern deep sub-micron era these networks are prone to many sources of noise hence making the voltage supply uctuate. This Vdd-Ground noise can have detrimental effect on design quality. This paper presents a unique strategy of achieving noise immunity through voltage scheduling in Data Flow Graphs (DFGs). A dynamic programming based approach is applied to obtain noise immunity by imposing a grid on the volt ...

Keywords: high-level noise-immune optimization

17 TSEM, a flexible scenario based small forces model
Bruce D. Link, Henry D. Shapiro
December 1979 **Proceedings of the 11th conference on Winter simulation - Volume 2**

Full text available: pdf(2.10 MB) Additional Information: full citation, abstract, references, index terms

An accurate computer model of a small force engagement is useful in evaluating the combat effectiveness of armed escorts for sensitive shipments, security guard forces and military patrols. The Transportation Safeguards Effectiveness Model (TSEM), primarily intended for, but not limited to, the study of ambushes of armed convoys, provides the user with considerably greater flexibility in directing the actions of the combatants than previous models. A user oriented script language is present ...

18 Task-specific visualization design: a case study in operational weather forecasting
Lloyd A. Treinish
October 1998 **Proceedings of the conference on Visualization '98**

Full text available: pdf(1.93 MB) Additional Information: full citation, references, citings, index terms
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Keywords: computational tracking, graphics design, meteorology, operational weather forecasting, perception, user tasks, visualization

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